

Prof. Sriram Venkatesh

PRINCIPAL

UNIVERSITY COLLEGE OF ENGINEERING (AUTONOMOUS)

Osmania University

A University with Potential for Excellence

A University Accredited by NAAC with A+ grade

Category - I Grade Autonomy by UGC

An ISO Certified Institution : ISO 9001 : 2015, 14001 & ISO 50001 : 2018



No.1508 /Admn./UCE OU/2023

Date: 13 .09.2023

Advertisement for Project Associate - I position in the MeitY sponsored Chip to Startup (C2S) Program in the Department of Electronics & Communication Engineering, University College of Engineering (A), Osmania University.

Applications are invited from eligible candidates to work as Project Associate - I in C2S Project titled "The Design, Fabrication and Development of Silicon Proven IP Core for High Resolution ADPLL"

Number of positions available: TWO (2)

Aim of the Project: Design, Fabricate and Develop Silicon Proven, IP Core for High Resolution All Digital Phase Locked Loop (ADPLL) suitable for Bluetooth Low Energy Applications.

For more information regarding the project, visit: <http://www.uceou.edu/pdfs/faculty/50022-ADPLL-IP-Core-C2S-MeitTy.pdf>

Qualification:

- First class in Bachelors degree in Electronics and Communication Engineering or equivalent/ ME/ M.Tech in Electronics and Communication Engineering or equivalent preferable in VLSI or related domains.
- GATE/UGC-NET qualified.
- Experience in Verilog HDL/VHDL, Analog IC Design and Cadence Virtuoso will be given preference.

Fellowship:

- Rs. 31,000 per month +HRA as per norms(for project tenure of maximum five years) for GATE/NET qualified candidates
- Rs. 25,000 per month +HRA as per norms(for project tenure of maximum five years) for other candidates

General Terms and Condition: The position is temporary and renewable each year subject to satisfactory performance for a maximum of five years.

Completely filled in, signed application form must be submitted as per the template provided (Annexure-I). Original documents of age proof/certificates/degrees/mark sheets and other testimonials must be presented at the time of interview. Attested photocopies of these documents will be collected at the time of interview. Only shortlisted candidates will be communicated through email to appear for the interview and no other communication in this regard will be entertained.

No TA/DA will be paid for attending the interview.

Completed applications should reach on or before 22nd September, 2023 via email addressed to: chandrashkar.p@uceou.edu



PRINCIPAL

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University College of Engineering

(AUTONOMOUS)
OSMANIA UNIVERSITY, HYDERABAD - 500 007.



ANNEXURE- I

APPLICATION FORM FOR POST OF PROJECT ASSOCIATE- I IN THE MEITY SPONSORED CHIP TO STARTUP (C2S) PROGRAM IN THE DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

1. Name in full (in BLOCK letters):
2. Parent's Name:
3. Date of birth :
4. Present address for correspondence:

Paste a recent
passport size
photograph

Mobile:
Email ID:

5. GATE/CSIR/UGC Exam : Y/N
(If Yes then give the percentage mark/rank and year of passing)

6. Educational Qualifications: (From SSC) (add more rows as required)

Sl. No	Qualification	Board/University	Year of passing	Percentage (%)

7. Experience:

Name of Post	Name of Organisation /Dept.	From	To	Nature of duties performed

8. Number of Publications in Journals / Conferences*:

9. Courses/Training in VLSI(provide proof):

DECLARATION

I hereby, undertake that all the details furnished above are true to the best of my knowledge and I am liable for any disciplinary action, if found otherwise. My candidature may kindly be considered for the above temporary/contractual/short-term project position as per the rules of UGC/DST/MietY.

Place:

Date:

Signature

INSTRUCTIONS:

1. The application form should be neatly typed and sent by e-mail (chandrasekhar.p@uceou.edu) so as to reach before the deadline i.e 22-09-2023.
2. *Enclose photo copies of certificates and reprints of published work.